Simulation and Benchmarking of Real Quantum Hardware

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The effects of noise are one of the most important factors to consider when it comes to quantum computing in the noisy intermediate-scale quantum computing (NISQ) era that we are currently in. Therefore, it is important not only to gain more knowledge about the noise sources appearing in current quantum computing hardware in order to suppress and mitigate their contributions, but also to evaluate whether a given quantum algorithm can achieve reasonable results on a given hardware. To accomplish this, we need noise models that can describe the real hardware with sufficient accuracy. Here, we present a noise model that has been evaluated on superconducting hardware platforms and could be adapted to other common architectures such as trapped-ion or neutral atom devices. We then benchmark our model by simulating a 20-qubit superconducting quantum computer, and compare the accuracy of our model to similar approaches from the literature and demonstrate an improvement in the overall prediction accuracy.

I. INTRODUCTION

Quantum computing is a promising candidate to solve complex problems in various fields such as optimization [1–4], quantum simulation [5–7], etc. much more efficiently than classical computers. However, the actual realization of quantum devices with a sufficient number of qubits to exploit the true potential of quantum computing is proving to be a major challenge.

There are various hardware realizations that are currently used to implement quantum computing units, with the most established realizations currently being superconducting qubits [8–10], ions [11–13] and neutral atoms [14, 15]. There are several other strategies, ranging from semiconductor qubits [16, 17] to more exotic approaches such as Majorana qubits [18, 19], yet it is not clear which will be the best solution in the long run.

All current realizations of quantum computers are still considered noisy intermediate-scale quantum (NISQ) devices [20–22], meaning that the hardware is noisy and can only be used for a limited number of error-prone operations before the quantum nature of the system vanishes [21]. Therefore, understanding, mitigating and suppressing the noise is one of the main focuses in the improvement of current quantum computers.

Due to the limited number of operations, it is not only necessary to evaluate the optimal hardware realization to tackle a specific problem on a quantum computer, but there is also a need to understand and characterize the noise [23, 24] in the devices in order to mitigate its effects [25, 26]. For both problems, good noise models that accurately describe the quantum device are crucial.

We validate our model by comparing the predictions to the results obtained from an IQM superconducting 20-qubit chip [27] and to the results already performed on IBM Q Melbourne [28]. The noise model described in this paper was implemented using the Eviden Qaptiva software framework, and the simulation was subsequently run on the Eviden Qaptiva system [29]. For the comparison itself, we used specific benchmark circuits varying in type (structured and random) and size (from 2 to 15 qubits and circuit depths ranging from 5 to 1062). This means that our model permits us to predict measurement results for arbitrary quantum algorithms running on real hardware. In both cases, we show that the results of the simulations are in good agreement with the results from real hardware.

We construct a general and holistic noise model that allows to describe noisy quantum computers with an arbitrary number of qubits and gates. Moreover, even though our model has been evaluated on superconducting devices, it can be adapted to different platforms by using different parameters, pertinent to that hardware. Adaptation to different hardware realizations can be easily achieved by feeding in the noise parameters of the respective hardware. The model itself is a combination of different error channels that are most likely to appear in all hardware realizations of quantum computers.

The paper is organized as follows: In Sec. II we describe the IQM 20-qubit chip used for the benchmarks. The associated noise model is discussed in Sec. III and the results of simulating the noise model against the real hardware are shown in Sec. IV. In Sec. V we present the conclusion of our work.

II. THE IQM 20-QUBIT CHIP

In this paper, the measurement results used to validate the simulation results were obtained from specific hardware. In particular, a superconducting 20-qubit chip fabricated by IQM was used to run the benchmark circuits

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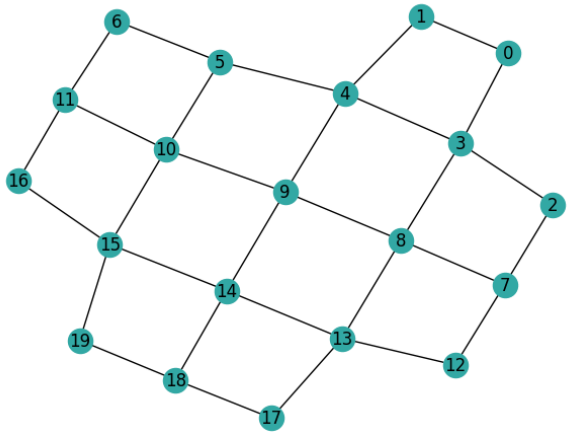

FIG. 1. Setup of the IQM chip used to benchmark the simulated results. Every node denotes a superconducting Transmon qubit. Tunable couplers between qubits are denoted by lines. The qubits are arranged in a square grid.

presented in Sec. IV.

Regarding the topology, the qubits are arranged in a square grid topology (see Fig. 1). Whenever a two-qubit gate is applied between non-neighboring qubits, a topology adaptation step (e.g., SWAP insertion [30]) is required. To reduce crosstalk between the qubits, tunable couplers are placed between all connected qubits [31]. These tunable couplers are also used to implement the native entangling gate - the `CZ` gate, described by the unitary:

$$\texttt{CZ} = \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & -1 \end{pmatrix}. \tag{1}$$

The single-qubit gate implemented on the hardware describes an arbitrary rotation of angle Θ around the $\cos(\Phi)\hat{\sigma}_x + \sin(\Phi)\hat{\sigma}_y$ axis on the Bloch sphere [32, 33]. The terms $\hat{\sigma}_x$ and $\hat{\sigma}_y$ represent the Pauli X and Y matrices defined as

$$\hat{\sigma}_x = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix}, \tag{2}$$

$$\hat{\sigma}_y = \begin{pmatrix} 0 & -i \\ i & 0 \end{pmatrix}, \tag{3}$$

and Φ represents the azimuthal angle on the Bloch sphere. Here the gate is denoted as $\texttt{PRX}(\Theta, \Phi)$ and its matrix representation is given by:

$$\texttt{PRX}(\Theta, \Phi) = \begin{pmatrix} \cos\frac{\Theta}{2} & -ie^{-i\Phi}\sin\frac{\Theta}{2} \\ -ie^{i\Phi}\sin\frac{\Theta}{2} & \cos\frac{\Theta}{2} \end{pmatrix}. \tag{4}$$

This gate is sometimes named differently in the literature, e.g. `R` in Qiskit [34] and `PhasedX` in pytket [35]. The two gates `PRX` and `CZ` form a complete gate set for the IQM quantum computing hardware [36].

Parameter	Mean	Median
$\mathcal{F}_{\texttt{1QB}}$	99.85 %	99.89 %
$\mathcal{F}_{\texttt{2QB}}$	98.59 %	99.06 %
$T_{\texttt{1QB}}$	20 ns	20 ns
$T_{\texttt{2QB}}$	40 ns	40 ns
T_1	41.8 μs	43.1 μs
T_2	3.2 μs	2.8 μs
ϵ^0_{meas}	2.66 %	2.43 %
ϵ^1_{meas}	5.09 %	3.63 %

TABLE I. Average noise parameters of the IQM 20-qubit chip, as measured during the calibration of the chip. Here, `1QB` denotes the single-qubit gate `PRX` and `2QB` denotes the two-qubit gate `CZ`. The average is taken over all connected qubit pairs for the two qubit gate fidelities and times. More details about the noise parameters can be found in App. A.

Like any quantum computing device, the IQM 20-qubit chip [24] is affected by noise. Noise is characterized by different noise parameters that must be determined for the respective hardware [37]. The characteristic quantities measured for the noise model, which have been obtained by performing coherence time measurements and randomized benchmarking experiments [38], are listed below:

- Single-qubit gate fidelity $\mathcal{F}_{\texttt{PRX}}$ and time $T_{\texttt{PRX}}$
- Two-qubit gate fidelity $\mathcal{F}_{\texttt{CZ}}$ and time $T_{\texttt{CZ}}$
- Relaxation time T_1
- Depolarization time T_2
- Measurement error probabilities for state 0 ϵ^0_{meas} and state 1 ϵ^1_{meas}

These parameters together with the corresponding gate durations are used as inputs for the the noise model, which implements a digital twin of the IQM 20-qubit chip. A detailed description of this procedure is given in Sec. III. In particular, all input parameters were determined for each qubit or qubit pair in order to obtain a more accurate simulation of the hardware. The average parameters used for the IQM 20-qubit chip are listed in Table IV. The parameters for all qubits and qubit pairs are given in App. A.

To gain further insight into the distribution of single- and two-qubit gate errors, as well as the readout errors, we consider the cumulative distributions of the single parameters, shown in Fig. 2. The details about the parameters obtained are given in [38].

III. THE NOISE MODEL

Quantum hardware is affected by noise due to interactions with the environment, miscalibration, errors in the control electronics, etc. For techniques such as error

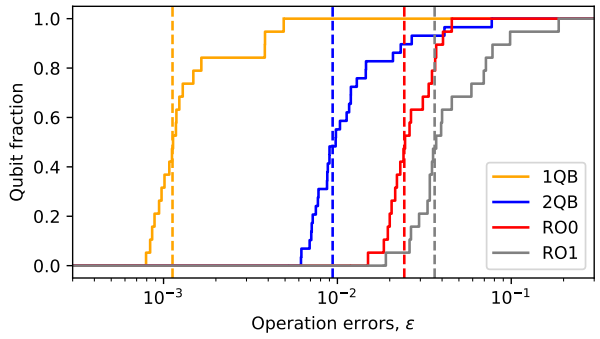

FIG. 2. Cumulative distribution of average single-qubit gate errors (1QB), two-qubit gate errors (2QB), readout errors of state 0 (RO0), and readout errors of state 1 (RO1) for the IQM 20-qubit QPU with vertical lines indicating median values.

mitigation, it is important to have an accurate model of the corresponding errors in the quantum hardware. Furthermore, a good hardware simulation model is essential for benchmarking current hardware and for evaluating whether certain algorithms run with a reasonable quality on the device. Here we describe a noise model that was originally intended to model the IQM superconducting hardware described in Sec. II, but can be adapted to be used on any other common quantum hardware implementation (e.g. ions, neutral atoms, etc.) by changing the respective noise parameters.

In order to balance the accuracy and generality of the noise model, we focus on noise channels (see next section) that typically appear in most current quantum hardware. In the following subsections, we present and discuss the noise channels used in our model description.

Each quantum channel $\mathcal{E}$ described in Secs. III A-III D imposes a transformation of the density matrix $\hat{\rho}$ representing the quantum system (in this case, the state of the quantum register [37]),

$$\hat{\rho} \longrightarrow \mathcal{E}(\hat{\rho}). \tag{5}$$

The quantum map $\mathcal{E}$ has the properties of being linear, completely positive (CP), and trace-preserving (TP). These ensure that the properties of the density matrix which are necessary to describe valid quantum states are preserved.

We use the Kraus operator formalism [39] to describe the channel $\mathcal{E}$, i.e.

$$\hat{\rho} \to \hat{\rho}' = \sum_i \hat{K}_i \hat{\rho} \hat{K}_i^\dagger, \tag{6}$$

where K_i corresponds to the Kraus operators. In the next subsections, three different channels that are used within our noise model with their corresponding Kraus operators will be presented.

A. Energy Relaxation

Since the qubits of a quantum hardware are not perfectly isolated, there is always some residual interaction with the environment. One of the processes resulting from these interactions is referred to as amplitude damping [23, 40]. In this process, the energy of the qubit is transferred to its environment, leading to a decay of the qubit from its excited to its ground state. The typical characteristic quantity of these processes is called the T_1 time which denotes a characteristic time scale for a qubit to relax to the ground state under the influence of the environment. In our implementation, T_1 is also the input parameter of the model. A relaxation process with a characteristic timescale of T_1, is described by the following Kraus operators

$$\hat{K}_{r,0} = |0\rangle\langle 0| + \sqrt{1 - p_r(t)}\,|1\rangle\langle 1| \tag{7}$$

$$\hat{K}_{r,1} = \sqrt{p_r(t)}\,|0\rangle\langle 1|\,, \tag{8}$$

with $p_r(t) = 1 - \exp(-t/T_1)$ as the time-dependent relaxation rate and t, in the context of noise modeling, is determined by the duration of the operation whose noise we are describing with this process.

B. Dephasing

Another significant environmental factor that impacts qubits is dephasing. In this scenario, the qubit does not actively exchange energy with its environment, as observed in the relaxation case, but rather undergoes a decay in its phase information over time [23, 41]. This phenomenon can be attributed to the presence of a frequency background of the environment, resulting in time-dependent fluctuation of the qubit's characteristic frequency. This process leads to a damping of the off-diagonal elements of the density matrix, i.e. dephasing. It is important to note that relaxation also results in the dephasing of the qubit since relaxation to the ground state effectively destroys phase information as well. The characteristic quantity that describes the total dephasing is referred to as the T_2 time, which is defined as the average time it takes for a qubit to fully lose its phase information. This T_2 encompasses both the dephasing arising from relaxation processes and the pure dephasing component. The pure dephasing component is characterized by its own parameter, T_ϕ. The overall T_2 time combines the dephasing due to T_1 processes and the pure dephasing, and is given by $1/T_2 = 1/(2T_1) + 1/T_\phi$ [32]. Since the T_1 component of dephasing is already incorporated into the relaxation, we proceed to define the Kraus operators for the pure dephasing process, which is expressed as follows:

$$\hat{K}_{d,0} = \sqrt{1 - p_d(t)}\hat{\mathbb{1}} \tag{9}$$

$$\hat{K}_{d,1} = \sqrt{p_d(t)}\hat{\sigma}_z, \tag{10}$$

where $p_d(t) = 1 - \exp(-t/T_2)$, and $\hat{\sigma}_z$ is the Pauli Z matrix.

C. Depolarization

The quantum error channel employed in our model to describe gate errors is the so-called depolarization channel. A full tomographic characterization of the quantum channel of a gate is resource intensive [42]. Unlike randomized benchmarking, which is routinely performed as part of the calibration procedure, tomography is not routinely performed and therefore not necessarily available to the user. For lack of such tomographic information, we therefore choose to describe the errors of quantum gates with the quantum depolarizing channel that does not assume any predominance of an error (X, Y or Z) over another. It is defined as:

$$\hat{K}_{\text{dep},0} = \sqrt{1 - p_{\text{dep}}(t)}\hat{\mathbb{1}}, \tag{11}$$

$$\hat{K}_{\text{dep},1} = \sqrt{p_{\text{dep}}(t)/3}\hat{\sigma}_x, \tag{12}$$

$$\hat{K}_{\text{dep},2} = \sqrt{p_{\text{dep}}(t)/3}\hat{\sigma}_y, \tag{13}$$

$$\hat{K}_{\text{dep},3} = \sqrt{p_{\text{dep}}(t)/3}\hat{\sigma}_z, \tag{14}$$

with $\hat{\mathbb{1}}$ being the identity operator, the Pauli operators $\hat{\sigma}_x$ and $\hat{\sigma}_y$ defined in (2) and (3) and the Pauli Z operator $\hat{\sigma}_z$ defined as

$$\hat{\sigma}_z = \begin{pmatrix} 1 & 0 \\ 0 & -1 \end{pmatrix}. \tag{15}$$

We fix the depolarization probability to match the average error rates we introduced above. We also note that in the case of random circuits, the use of depolarizing noise instead of a more specific noise model is justified by the fact that averaging over random gates turns any noise channel into a depolarizing channel with equivalent average process error.

D. State Preparation and Measurement (SPAM) Errors

The last error we include in our modeling of noisy circuits is the error in the final measurement of the qubits. In particular, registering an erroneous result means falsely measuring the qubit in the ground state when it is actually in the excited state, or the opposite case of falsely measuring the excited state. Imperfect measurements in quantum devices are a very common source of error in current quantum architectures (see Fig. 2) and should be considered in a realistic modeling of quantum computing hardware. To model imperfect measurements, we replace the perfect projective quantum measurements by imperfect positive operator-valued measures (POVMs) in our model of the circuit [37]. The measurement on each qubit is thus described by a pair of positive semi-definite operators $\hat{E}$ and $\mathbf{1} - \hat{E}$ with respective outcomes 0 and 1. The probability of measuring the wrong result for a qubit in state $|0\rangle$ or $|1\rangle$ is denoted by ϵ^0_{meas} or ϵ^1_{meas}, respectively. Within our noise model, we neglected initialization or state preparation errors because these errors are generally difficult to track and – at least during our studies – did not show any major differences in our results when included. Consequently, we decided not to include this source of error and to consider only measurement errors for our noise model.

E. Modeling Noisy Circuits

In the last subsection, we presented the building blocks for our noise model. To actually model a circuit executed on real noisy quantum computing hardware, we need to assemble these building blocks together.

The time evolution of the system is determined by applying the respective noise channels. The specific choice in which to apply them is the main characteristic of the respective noise model. The construction of the noise model is as follows:

- For each gate, the depolarizing channel is applied for the gate time t_g, where the error is characterized by the gate fidelity obtained from the hardware (measured via randomized benchmarking [43–46]).
- During the idle time of the qubit, i.e. when no gate is applied to the qubit, the relaxation and dephasing channels are applied to the qubit, characterized by T_1 and T_2, which are obtained from the hardware.
- At the very end of the circuit we apply the measurement channel including measurement errors, where again the measurement error parameters $\epsilon^{0/1}_{\text{meas}}$ are measured in the hardware.

A schematic description of our noise model, i.e. how a noiseless circuit is transformed into a noisy circuit, can be found in Fig. 3.

Georgopoulos et al. [28] present a comparable approach to simulate superconducting hardware by IBM. The main difference between our model and theirs is that in their model after a gate, the depolarizing channel is applied first and afterwards the relaxation and dephasing channels are applied to simulate idle noise. We apply these two channels during the idle time of the qubit, meaning the depolarizing channel is only applied for gate errors while relaxation and dephasing occurs only on idle qubits. From our point of view, this seems to be a physically more reasonable approach. The results presented in the next section also provide strong evidence for this assumption. The described noise model and all simulations presented in the next section were run on the Eviden Qaptiva 1.11.2, a quantum programming and simulation platform [29].

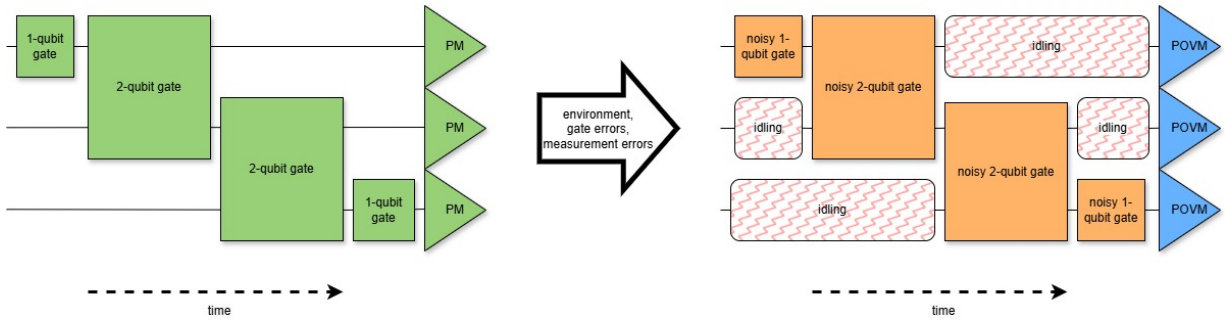

FIG. 3. Transition from an ideal to a noisy circuit used in our simulations. Each noiseless gate (solid boxes) is transferred to a quantum channel that includes the effect of the gate and the depolarization error. When the qubit is in the idle state (zigzag boxes), the relaxation and dephasing channel is applied and the projective measurements (triangles) of the noiseless circuit are replaced by a more general POVM accounting for the measurement errors.

IV. NOISE MODEL COMPARISON TO REAL HARDWARE

In this section we compare our noise model with measurement results obtained on a real IQM 20-qubit hardware (see Sec. II). For the comparison, we choose several benchmark circuits varying from very small (5) to rather large (> 100) circuit depths.

A. Comparison Metric: The Hellinger Distance

For a quantitative comparison, we need reasonable metrics to compare the probability distribution measured in the experiment with the one resulting from the simulation of our noise model. A widely used mathematical metric to compare the similarity of probability distributions is the Hellinger distance [47]. The Hellinger distance for two probability distributions $P = \{p_i\}$ and $Q = \{q_i\}$ can be computed as follows:

$$h(P,Q) = \frac{1}{\sqrt{2}}\sqrt{\sum_{i}^{n}(\sqrt{p_i} - \sqrt{q_i})^2}, \tag{16}$$

where n is the number of discrete categories (bitstring outcomes) in the probability distribution. The Hellinger distance assumes values in the range of $[0, 1]$. A Hellinger distance of zero represents a perfect overlap between two distributions. Another important property of the Hellinger distance is that it doesn't require the distributions P and Q to have the same support. The support of a distribution is defined as the subset of the distribution function domain with non-vanishing probability values. This property ensures that reasonable distance values can be obtained even when the probability mass of one distribution is concentrated around a few data points. This scenario is relevant to GHZ states where the noiseless distribution assumes equal probability values for only two bitstring outcomes, while the noisy GHZ histogram attains a more smeared-out distribution for all states. The Hellinger distance effectively accounts for outcomes with noiseless zero-probability contributions, a feature that the classical fidelity neglects. Thus, the Hellinger distance will be used in the following to evaluate the quality of our simulation results compared to the real measured ones.

B. Benchmark Circuits

With our model, we aim to accurately describe the execution of noisy circuits of different depths. Therefore, we chose a variety of benchmark circuits to evaluate the accuracy of our noise model, including small, medium, and large circuits. Moreover, we used both random and structured circuits to avoid any bias due to the simplification of the noise occurring in random circuits [48] and to show that our model describes structured circuits as well. The circuits already match the target gate set of the associated hardware (see. Sec. II), i.e. contain only `PRX` and `CZ` for the IQM QPU, and `U1`, `U2`, `U3` and `CNOT` for IBM Q Melbourne.

To generate these benchmark circuits, a compiler was employed to transform the initial logical circuits into circuits with an adapted topology and gateset. An example is shown in Fig. 5. As illustrated, the GHZ-4 circuit, comprising of one Hadamard gate `H` and three `CNOT` gates was transformed. As a first step, the circuit's topology has been adapted to the QPU by using a SWAP-insertion ansatz [49], which has been implemented using Eviden's Qaptiva framework and is referred to as Nnizer [50]. As a final step, the compiler translates all non-native gates, such as the `H` and `CNOT` gate, to native gates of the QPU, i.e. `PRX` and `CZ` gates.

In particular, the benchmark circuits themselves can be divided into four classes: Greenberger-Horne-Zeilinger (GHZ) circuits [51] for two to seven qubits, a random unitary (RU) circuit and one QAOA circuit for the IQM device, and quantum walk circuits for four to fifteen qubits [52] for IBM Q Melbourne. For GHZ circuits starting at eight qubits, we observed that the quality of the

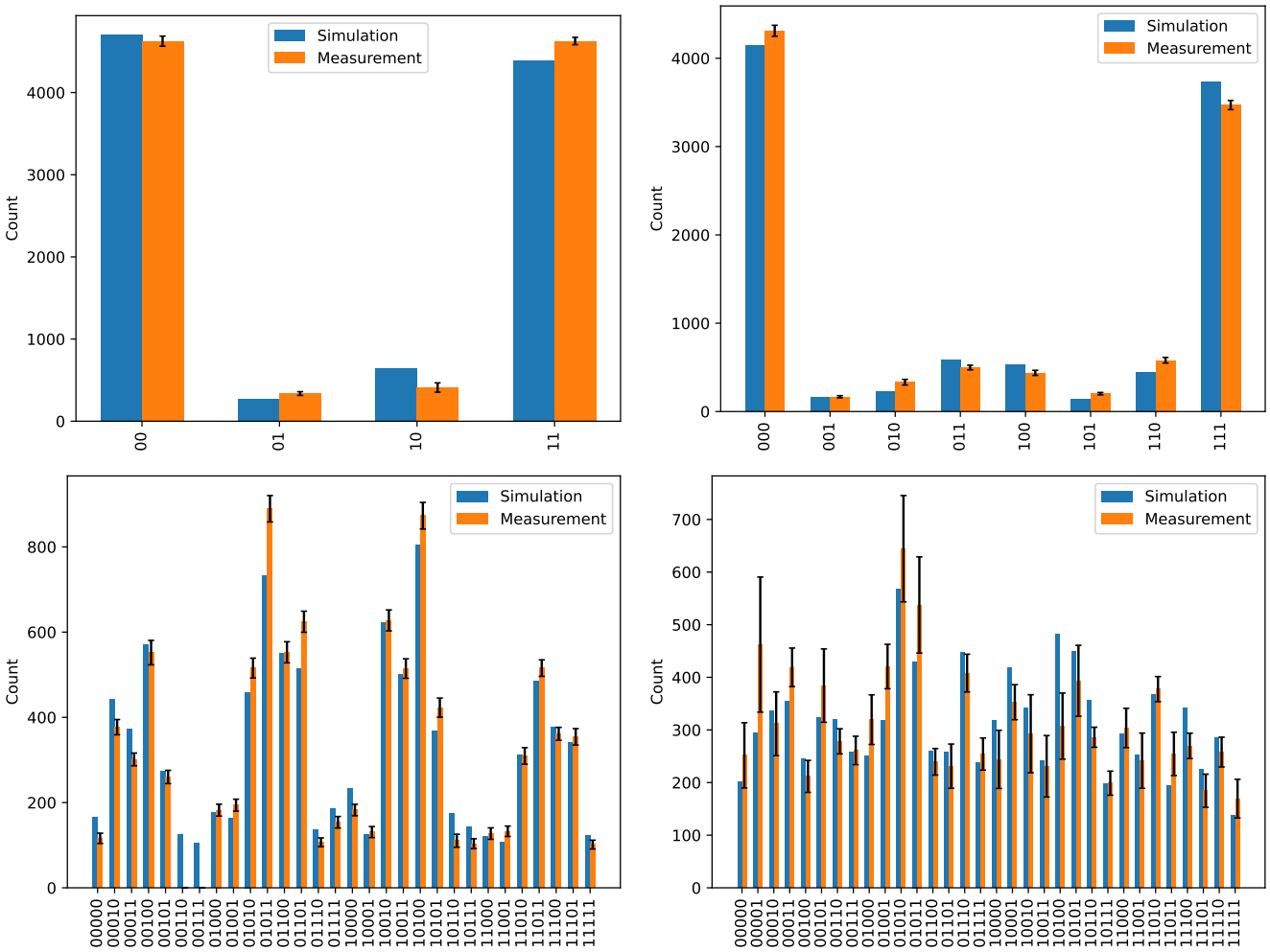

FIG. 4. Comparison of the results of our noise model simulations and the measurement results obtained on the IQM 20-qubit QPU for different classes of circuits: GHZ-2 (top left), GHZ-3 (top right), RU (bottom left), QAOA (bottom right). To get the simulated results, a deterministic simulation was performed which generates a probability distribution for all states. The state probabilities have then been multiplied by 10,000 to get the counts. The results on real hardware were obtained by repeating 10,000 circuit executions (shots) 50 times. The blue bars show the counts obtained from the simulation for the respective states, and the orange bars show the counts measured in the experiment. The error bars represent the standard deviations due to finite sampling. States with counts below 100 have been neglected for visualization reasons.

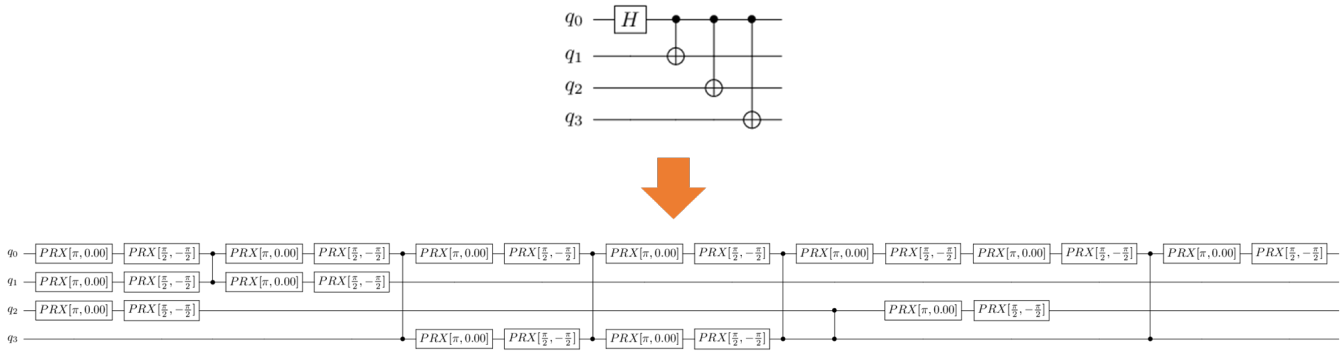

FIG. 5. Compilation of an input GHZ-4 circuit (top) into an IQM-compatible circuit (bottom). The circuit was translated using a compiler designed for the IQM-20-qubit QPU.

Circuit	Qubits	Depth	1QB Gates	2QB Gates
GHZ-2	2	5	6	1
GHZ-3	4	16	22	5
GHZ-4	4	19	26	6
GHZ-5	5	20	30	7
GHZ-6	6	36	46	11
GHZ-7	7	46	62	15
RU	5	33	48	13
QAOA	5	87	110	37
QW-2 [52]	4	44	19	35
QW-3 [52]	6	194	83	178
QW-4 [52]	11	409	175	423
QW-5 [52]	14	733	297	811
QW-6 [52]	15	1062	449	1137

TABLE II. The number of qubits, circuit depth, and the number of single-and two-qubit gates for the benchmark circuits investigated during this work.

measurements began to decrease, and comparing them to our noise model would no longer make sense. The main circuit resources per benchmark circuit are listed in Table II. The circuit representations for each benchmark circuit are linked in App. B.

C. Results

1. *GHZ, random unitary and QAOA circuits*

In this section, we will compare the simulation results of our noise model with the ones obtained from the real IQM quantum computing hardware as presented in Sec. II. For the purpose of our comparison, we will be using the circuits described in Sec. IV B and the Hellinger distance as a quantitative measure of agreement (see Sec. IV A). The real measurement results were obtained by running each circuit on the IQM hardware for 10,000 times to obtain the respective probability distribution, i.e., the probabilities associated with the final quantum states.

The simulation results were obtained by implementing the noise model described in Sec. III using the Qaptiva software framework and subsequently simulating it on emulators included in Qaptiva.

To ensure a realistic comparison, a deterministic simulation yielding a probability distribution for every single state has been used. To get an exact comparison with the hardware results, we then multiplied the probability of every single state by 10,000. The histograms illustrating the outcomes of both the simulations and the measurements are presented in Fig. 4 for two GHZ circuits, one random unitary and one QAOA circuit. A comprehensive summary of the respective Hellinger distances is provided in Table III.

Both the histograms and the Hellinger distances show good agreement between our noise model and the actual

Circuit	Hell. dist.
GHZ-2	0.040
GHZ-3	0.044
GHZ-4	0.055
GHZ-5	0.073
GHZ-6	0.115
GHZ-7	0.104
RU	0.055
QAOA	0.071

TABLE III. Hellinger distances for the benchmark circuits performed on the IQM 20-qubit QPU and averaged over a total of 50 measurements.

experimental data. Especially for the smaller circuits – namely GHZ-2 to GHZ-5 – the agreement of the results is almost perfect with Hellinger distances below 0.1. For GHZ-6 and GHZ-7 the noise model still accurately reflects the real hardware, with the worst Hellinger distance of 0.115 for the GHZ-6 circuit. The random unitary and QAOA circuit again show Hellinger distances well below 0.1, highlighting that even for larger circuit depths, our noise model matches very well with the measurements performed on the real hardware. Note that for the QAOA circuits, the hardware outputs are close to random sampling due to the large depth of the circuits. However, our simulations nicely reflect this behavior, proving that the noise model is capable of simulating very large and noisy circuits and giving good evaluations of the result quality of the real hardware.

We also observe discrepancies between the simulated and measured data. An example is the asymmetry of the target state for the GHZ-3 results (Fig. 4 top right), which is not resolved as strongly by the simulation as it is in the real hardware. For the QAOA circuit (Fig. 4 bottom right) the probability distribution is biased towards lower excitation states in the measurement, which is not reproduced as strongly in the simulation. These deviations between simulation and real data are most likely due to more complex noise sources. The most reasonable candidates for superconducting hardware are coherent errors (e.g. overrotations), leakage out of the computational subspace, and crosstalk [24].

However, an analysis of the results of [28] reveals that our noise model outperforms competing models when comparing different noise models. This is evident in all circuit sizes, particularly when utilizing calibrated hardware parameters instead of fitted ones. These findings demonstrate the efficacy of our model in accurately simulating real quantum computing hardware for circuits of varying depths. These results will be presented in the next subsection.

2. *Comparison to other noise models*

To gain more insight into whether our proposed noise model performs well, we also made a comparison with an-

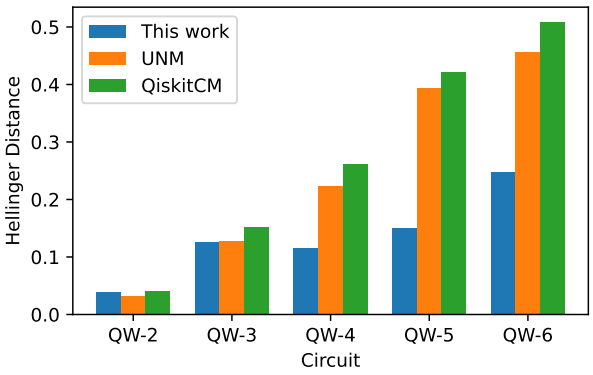

FIG. 6. Hellinger distances for the quantum walk circuits from this work and [28] that have been measured on IBM Q Melbourne. We compare our approach with the unified noise model (UNM) and the Qiskit composite model (QiskitCM). The Hellinger distances for the latter two models were taken from [28].

other approach, namely the so-called unified noise model (UNM) [28]. We studied the same circuits and implemented an emulated version of IBM Q Melbourne, with a native gateset consisting of `U1`, `U2`, `U3` as the single-qubit gates and `CNOT` as the native two-qubit gate. The noise parameters for this QPU are listed in Table IV. This way, we are able to compare our noise model with the results obtained with the UNM. In addition, we take the Qiskit composite model, which has also been studied in [28], as a further noise model for our benchmark analysis.

Fig. 6 shows the results for the Hellinger distances for the quantum walk circuits. Comparing these values with the noise models presented in [28] – such as the UNM and the Qiskit composite model – we can see that the two only circuits for which our proposed approach performs similarly is the 2- and 3-qubit quantum walk (QW-2 and QW-3) when compared to the UNM and the Qiskit composite model, whereas for all other cases (4- to 6-qubit quantum walks, i.e. QW-4, QW-5 and QW-6), we can see a good improvement of about 50%. An explanation for this observation could be that, especially for larger circuits, setting the relaxation and dephasing channel to simulate idle noise only on idle qubits might be a better approach.

In Fig. 8 of App. C, the counts of the measurements performed on IBM Q Melbourne and the counts obtained from the noise model for the quantum walk circuits are presented. Specifically, for the 2-, 3-, and 4-qubit quantum walk circuits (QW-2, QW-3, and QW-4), there is a substantial agreement between the measurement and simulation results. However, for the more complex circuits – namely QW-5 and QW-6 – with depths exceeding 700 and 1000, respectively, the Hellinger distance increases. This is completely expected as any discrepancy between the model and experiment is amplified for the longer circuits. As illustrated in the lower graph depicting the QW-6 circuit in Fig. 8 of App. C, there is a substantial count for the all-zero state, while the simulation indicates a significantly lower count. Despite this discrepancy in the all-zero state, simulation and measurement outcomes are in good agreement for all other states.

Parameter	Avg. value
$\mathcal{F}_{\texttt{1QB}}$	99.99 %
$\mathcal{F}_{\texttt{2QB}}$	96.83 %
$T_{\texttt{1QB}}$	100 ns
$T_{\texttt{2QB}}$	500 ns
T_1	56.15 μs
T_2	56.01 μs
ϵ^0_{meas}	7.61 %
ϵ^1_{meas}	7.61 %

TABLE IV. Average noise parameters for IBM Q Melbourne. Here, `1QB` denotes the single-qubit gates `U1`, `U2` and `U3`, where `2QB` denotes the two-qubit gate `CNOT`. The single- and two-qubit gate times $T_{\texttt{1QB}}$ and $T_{\texttt{2QB}}$ have been taken from [53]. All other noise parameters have been taken from [28].

V. CONCLUSION

In this work, we present a noise model that can describe many common gate-based quantum computing hardware platforms by using the typical noise parameters supplied by quantum hardware vendors. We evaluated the accuracy of our model by comparing the simulation results of our noise model with the measurement results of a 20-qubit superconducting quantum computing hardware. Furthermore, we compared our noise model to the one developed by Georgopoulos et. al. [28] and demonstrated that, particularly for large circuits with depths greater than 400, we could reduce the Hellinger distances by about 50%. In addition, we have shown that the simulations predict the behavior of real hardware in a truthful way for different types of circuits and depths. We attribute this increase in performance to a more accurate modeling of the noise on idling qubits.

Subsequent studies should explore the incorporation of more advanced error channels that yield minor discrepancies between simulation and real results. The noise model can be used for the evaluation and optimization of quantum algorithms prior to their execution on actual quantum computing hardware. Additionally, it can serve as a robust noise model for applications such as error mitigation.

In the near future, one could try to improve the presented noise model further by including for instance crosstalk and leakage at the gate level. Additionally, a study of this noise model on different architectures, such as trapped-ion or neutral atom quantum computers should be performed.

Qubit No.	$\mathcal{F}$ (%)	T_1 (μs)	T_2 (μs)	ϵ^0_{meas} (%)	ϵ^1_{meas} (%)
0	99.51	39.3	1.8	3.10	9.85
1	99.94	63.4	3.1	2.45	1.90
2	99.89	42.7	4.8	2.65	3.95
3	99.85	43.5	2.9	3.65	5.90
4	99.89	46.0	2.4	2.05	3.40
5	99.91	49.3	2.5	2.00	2.65
6	99.62	55.4	1.9	2.60	3.50
7	99.90	36.1	3.0	1.95	2.60
8	99.88	33.1	2.1	2.20	4.55
9	99.90	47.0	5.1	3.70	3.70
10	99.87	34.8	2.6	1.85	6.95
11	99.91	64.9	4.7	4.55	7.15
12	99.89	23.1	5.5	1.20	3.30
13	99.92	45.8	2.1	1.50	1.85
14	99.62	7.0	1.8	3.50	7.80
15	99.91	46.3	5.0	3.35	4.00
16	99.88	46.8	2.7	4.05	18.75
17	99.88	35.1	3.1	2.15	3.55
18	99.92	39.5	4.9	2.30	3.40
19	99.84	36.4	1.9	2.40	2.95

TABLE V. Single-qubit gate parameters (fidelity $\mathcal{F}$, relaxation time T_1, depolarization time T_2 and measurement errors for state 0 and 1 $\epsilon^{0/1}_{\text{meas}}$) for all qubits of the IQM 20-qubit chip. The single-qubit gate time is set to $T_{\texttt{PRX}} = 20\,\text{ns}$ for all qubits.

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Appendix A: Noise Data for the IQM 20-Qubit Chip

Table V and Table VI give more information about the noise parameters on each qubit and each qubit pair.

Appendix B: Benchmark Circuits

As mentioned above, we investigated the behavior of our noise model by benchmarking different types of circuits, namely a set of GHZ circuits, a random unitary circuit and a QAOA circuit. These circuits in QASM format can be found on https://zenodo.org/records/16082428.

Appendix C: Results for different Benchmark Circuits

In this section, we present the results obtained from the simulated and real QPUs. Fig. 7 shows the simulations of the circuits GHZ-4 to GHZ-7, while Fig. 8 highlights the results for the quantum walk circuits QW-2 to QW-6.

Qubit Pair	$\mathcal{F}$ (%)
0, 1	99.29
0, 3	99.02
2, 3	95.87
2, 7	99.13
1, 4	99.31
3, 4	97.32
3, 8	98.80
7, 8	99.22
7, 12	99.10
4, 5	99.38
4, 9	99.23
8, 9	99.38
8, 13	99.12
12, 13	99.28
5, 6	99.47
5, 10	99.13
9, 10	99.25
9, 14	98.71
13, 14	98.83
13, 17	99.10
6, 11	97.69
10, 11	92.28
10, 15	98.81
14, 15	98.54
14, 18	98.54
17, 18	99.02
11, 16	97.91
15, 16	99.29
15, 19	98.87
18, 19	98.97

TABLE VI. Two-qubit gate parameters (fidelity $\mathcal{F}$) for all qubits pairs of the IQM 20-qubit chip. The two-qubit gate time is set to $T_{\texttt{CZ}} = 40\,\text{ns}$ for all qubits.

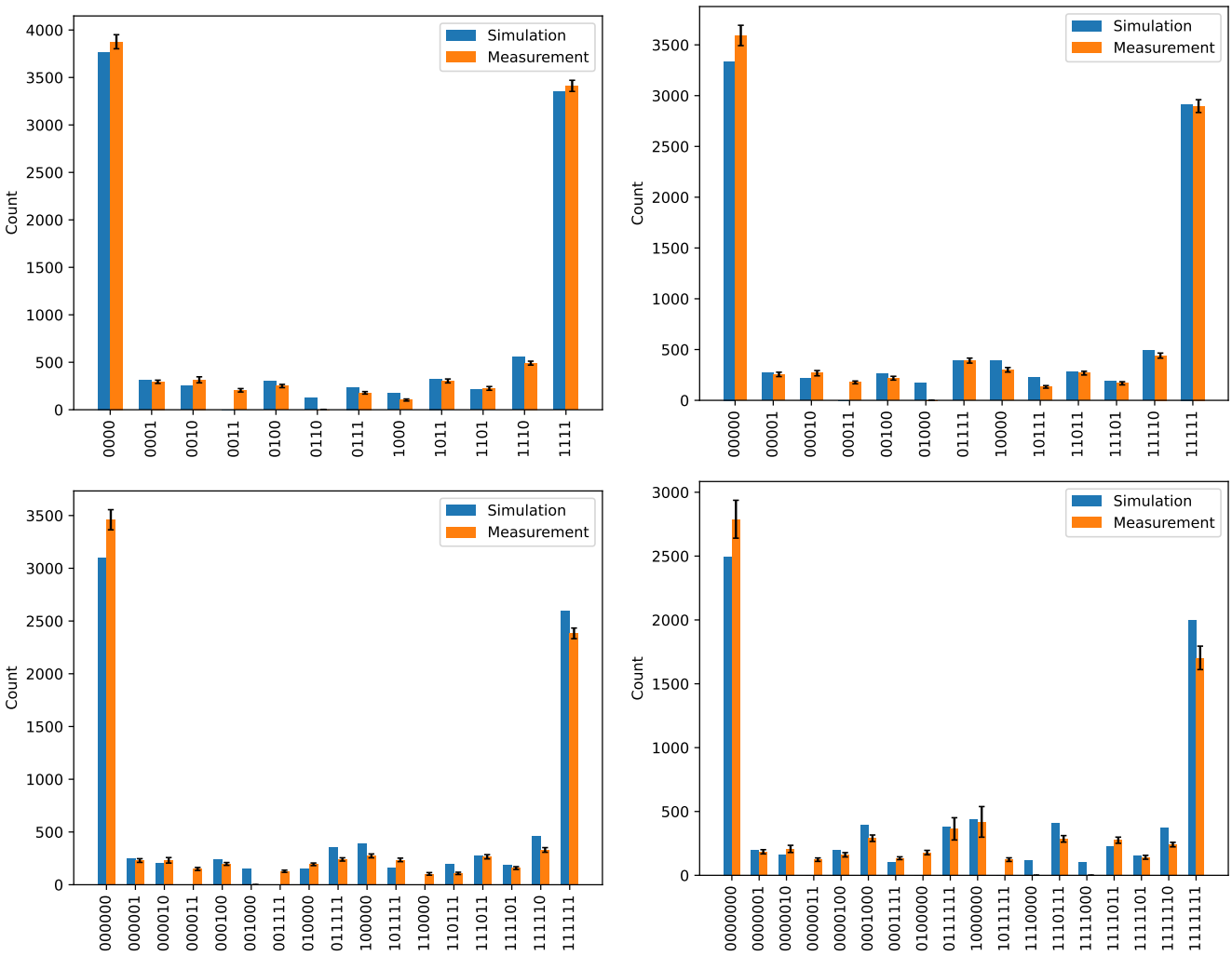

FIG. 7. Comparison of the results of our noise model simulations and the measurement result obtained on the IQM 20-qubit QPU for the GHZ circuits: GHZ-4 (top left), GHZ-5 (top right), GHZ-6 (bottom left), and GHZ-7 (bottom right). To get the simulated results, a deterministic simulation was performed which generates a probability distribution for all states. The state probabilities have then been multiplied by 10,000 to get the counts. The results on real hardware were obtained by repeating 10,000 circuit executions (shots) 50 times. The blue bars show the counts obtained from the simulation for the respective states, and the orange bars show the counts measured in the experiment. The error bars represent the standard deviations occurring from the repetitions of the measurements. States with counts below 100 have been neglected for visualization reasons.

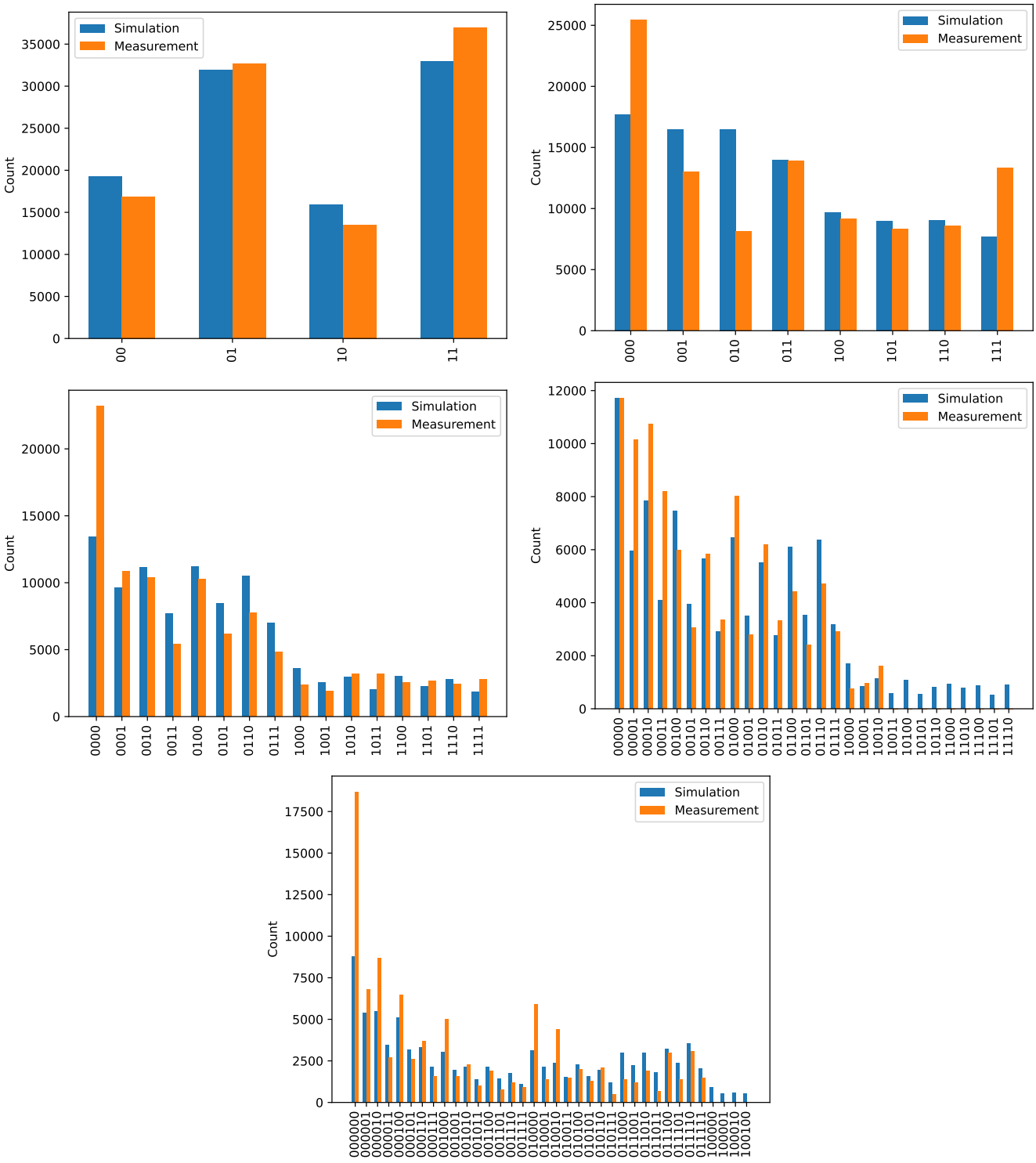

FIG. 8. Comparison of the results obtained from our noise model simulations and the measurement result obtained from IBM Q Melbourne for quantum walk circuits: QW-2 (top left), QW-3 (top right), QW-4 (center left), QW-5 (center right), and QW-6 (bottom). Both simulation and measurement results were obtained using 100,000 circuit executions (shots). The blue bars show the counts obtained from the simulation for the respective states and the orange bars the counts obtained from the real QPU. In this case, the uncertainties of the experimental results are in the order of approximately 100 shots and are therefore not visible in the plots. States with counts below 500 have been neglected for visualization reasons. The measurement data was taken from [28].

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